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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,604	08/07/2001	Friedrich Hapke	DE 000118	1419

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	7

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/923,604	HAPKE, FRIEDRICH	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *1-3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1-1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-3 are presented for examination.

Drawings

1. The drawings are objected to because Figure 2 refers to the multiplexor selector signal as PI5s, but the examiner believes that the signal should be PISs. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because there are several misleading and indefinite recitations, as follows:

a. Lines 8 and 11 refer to a "test circuit (2,3,4,5)" and then to a "buffer memory (2,3,4,5)", with the same reference of 2,3,4,5. The applicant needs to clarify which of the two is the correct naming, and then name both references the same.

b. Lines 9 and 11 are also indefinite, in that "a test sample" in line 9 seems to be applied for a second time ("this test sample") in line 11. The applicant should clarify or correct this statement, because the present wording is indefinite.

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: Page 5, line 27 refers to Fig.1, but the examiner believes that it should refer to Fig.2. Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: Page 6, line 7 refers to "PIs", but the examiner believes that it should refer to "PI". Appropriate correction is required.

5. The disclosure is objected to because of the following informalities: Page 6, line 9 refers to "PISs", but there is no such reference in Fig.2. Either the drawing of Fig.2 must be changed to incorporate "PISs" (see Drawing objection in paragraph 1 above), or this reference to "PISs" must be changed to match the drawing. Appropriate correction is required.

6. The disclosure is objected to because of the following informalities: Page 6, line 18 refers to "the test output TESTs", but the examiner believes that it should read "the test output TO". Appropriate correction is required.

Claim Objections

7. Claims 1-3 are objected to because of the following informalities: references placed in parenthesis in a claim are not given patentable weight. The elements that are within parenthesis in the three claims should be either further defined, or the parentheses should be removed. Appropriate correction is required.

8. Claims 1 and 3 are objected to because of the following informalities: The claims 1 and 3 are in violation of 37 CFR paragraph 1.75, paragraph (i); "Where a claim sets

forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.". The examiner requests that the applicant indent the separate elements of each claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim1 line 8, "a test circuit (2,3,4,5)" is recited, and then in line 10, "a buffer memory (2,3,4,5)" is recited, both of which the examiner believes are referring to the same elements in the drawing and specification. Reference to two different names for the same element renders the claim indefinite. This claim should name the referenced element once only.

11. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 8 of the claim recites "applies a test sample in a first test clock cycle", and then in line 10 recites "feeds back this test sample in a second test clock cycle". The recitations alone would lead the examiner to believe that the first and second clock cycles both receive the same test sample, but which is not the case. This application of a same test sample twice in the claim is not clear, and is indefinite in that

a person with ordinary skill in the art might interpret this wrongly, rendering the claim to be without function.

12. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 3 line 7, "a test circuit (2,3,4,5)" is recited, and then in line 10, "a buffer memory (2,3,4,5)" is recited, both of which the examiner believes are referring to the same elements in the drawing and specification. Reference to two different names for the same element renders the claim indefinite. This claim should name the referenced element once only.

13. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 8 of the claim recites "applies a test sample in a first test clock cycle", and then in line 10 recites "feeds back this test sample in a second test clock cycle". The recitations alone would lead the examiner to believe that the first and second clock cycles both receive the same test sample, but which is not the case. This application of a same test sample twice in the claim is not clear, and is indefinite in that a person with ordinary skill in the art might interpret this wrongly, rendering the claim to be without function.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Design of Scan-Based Path Delay Testable Sequential Circuits", Pramanick et al., October 17-21, 1993, IEEE, International Test Conference, pp 962-971. Pramanick et al., proposes a technique to produce robust path delay testable designs (see Abstract of text) on scan-based sequential circuits as is claimed by the applicant. A combinational logic circuit (see Pramanick et al., Figures 2 and 3) similar to the applicant's, has a test sample applied, and then re-applied through an iterative logic feedback as specified by the applicant, and then is sampled for proper behavior responses of this combinational logic system. Pramanick et al. teaches in the paper both theorem and proof of a robust delay test wherein a two-pattern test of the form <V1, V2> (see Pramanick et al. Definition 1 on page 963, and Theorems 1 and 2 on page 966) produces "100% robust path delay testability" (Pramanick et al. page 971). Pramanick et al. sets up the inputs, applies the vectors, and clocks the feedback iteratively in the same manner as does the applicant. The results of this test are compared to deterministic models using binary

decision diagrams and techniques as per Pramanick (see page 963, 2.2 BDDs and Logic Networks). In applying and clocking, Pramanick however uses a 2-stage latch arrangement that is commonly used for scanning data in some commercial applications, and so does not specifically call for a "buffer memory" as does the applicant. However, a person with ordinary skill in the art at the time of the invention would recognize that a group of latches performs the very same function as a buffer memory. Since Pramanick et al. uses latches, and since the applicant's specification for a buffer memory is broad, one would be motivated to apply Pramanick et al. by using a buffer memory of any manufacture instead of latches, since they are functionally identical, in order to duplicate the Pramanick et al. two-pattern test.

17. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Design of Scan-Based Path Delay Testable Sequential Circuits", Pramanick et al., October 17-21, 1993, IEEE, International Test Conference, pp962-971, as applied to claim 1 above. The paper by Pramanick et al. specifically teaches the use of latches in an LSSD design, which scan in test sample vectors, and which are used for the application of test samples (vectors) to the logic inputs of the circuit under test (see page 968, 3.2 Test Application). This arrangement by Pramanick is precisely the same as the claim by the applicant, therefore the applicant's claim is rejected.

18. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Design of Scan-Based Path Delay Testable Sequential Circuits", Pramanick et al., October 17-21, 1993, IEEE, International Test Conference, pp962-971, as applied to claim 1 above. In this analogous art of Pramanick et al., the method by which the testing is applied, and

circuit arrangement as well, are presented in a manner which does not fully teach all facets of the applicant's claim, and this disparity is shown in claim 1 above (paragraph 16). Just as there is motivation in claim 1 above, there too is the same in the rejection of this claim by the applicant. This claim is therefore rejected as being obvious.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
for
Albert DeCady
Primary Examiner